ABSTRACT OF THE DISCLOSURE

Methods and apparatuses to design an Integrated Circuit (IC) with a shielding of wires. In at least one embodiment of the present invention, a shielding mesh of at least two reference voltages (e.g., power and ground) is used to reduce both the capacitive coupling and the inductive coupling in routed signal wires in IC chips. In some embodiments, a type of shielding mesh (e.g., a shielding mesh with a window surrounded by a power ring, or a window with a parser set of shielding wires) is selected to make more routing area available in locally congested areas. In other embodiments, the shielding mesh is used to create or add bypass capacitance. Other embodiments are also disclosed.